IN THE SPECIFICATION

The following paragraphs are rewritten pursuant to 37 C.F.R. §1.121.

1. Replace the paragraph beginning at page 10, line 22 of the specification with the following paragraph:

With N-well 15 and device body 17 formed, the fabrication method next includes applying thin dielectric layer 28 and then the material for anode 30. These steps correspond to the steps of applying the gate insulation layer and gate electrode material, respectively, in transistor devices elsewhere on chip 11, and are performed concurrently with those steps. The areas other than the areas of chip 11 where lateral regions 20 and 22, and first end region 24 are to be located, are then masked off and N-type impurities are implanted in the exposed areas to form these regions. This step corresponds to the step of producing the source and drain regions in N-type transistor structures at other locations on chip 11 and is performed concurrently with that step. It will be appreciated that the silicon oxide layer previously deposited over the entire chip surface preferably remains in place during the formation of lateral regions 20 and 22, and first end region 24. The N-type impurity may be driven through the thin silicon oxide layer to be implanted in the underlying N-well silicon. However, alternative fabrication arrangements may remove the thin oxide layer or perform other steps at this point such as producing lightly doped regions corresponding with the lightly doped drain regions formed in transistor structures on chip 11.

Respectfully submitted,

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CERTIFICATE OF FACSIMILE

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office, (Fax No. 703-746-4000 on March 24, 2004.

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